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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Arnold M. FRISCH

Art Unit: 2138

Application No: 10/646,957

Examiner:
Dipakkumar B. Gandhi

Filed: August 21, 2003

For: PROGRAMMABLE JITTER GENERATOR

TRANSMITTAL OF BRIEF ON BEHALF OF APPELLANT

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Notice of Appeal was filed in this case on July 11, 2006.

Submitted herewith in triplicate is Appellant's Brief.

A check in the amount of $500 for the fee under 37 CFR 41.20(b)(2) is enclosed.

Respectfully submitted,

Daniel J. Bedell
Reg. No. 30,156

SMITH-HILL & BEDELL, P.C.
16100 N.W. Cornell Road, Suite 220
Beaverton, Oregon 97006

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: CRED 2779
Postcard: 08/06-8

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Sir:

Real Party In Interest

Credence Systems Corporation

Related Appeals And Interferences

None

Status of Claims

Claims 1-35 are pending.

Claims 1-35 are rejected.

No claims have been withdrawn.

Status of Amendments

No amendment was filed subsequent to final rejection.

Summary of Claimed Subject Matter

Each edge of a digital signal occurs at a point when its voltage crosses a particular threshold level. Although edges should occur at predictable times relative to edges of a periodic clock signal used as a timing reference when the digital signal was generated, noise can cause edge timing to vary. Variation in edge timing is called

"jitter". Since ICs are supposed to be resistant to some amount of jitter in the digital input signals they process, an IC can be tested for its resistance to jitter by determining whether it behaves properly when a controlled amount of jitter is added to its input. The applicant's invention relates to an apparatus for producing a jittery test signal for use in an IC test.

Claims 1 and 22

Claim 1 recites an apparatus 41 (see FIG. 4) comprising a programmable delay circuit 44 that delays a "first signal" (VIN) to produce a test signal (TEST) for use in an IC, and "first means" (pattern generator 46) for supplying a sequence of digital data words (DELAY) to the programmable delay circuit 44 for varying its delay so that the TEST signal jitters relative to the first signal VIN.

Apparatus claim 1 and method claim 22 includes analogous.

Claims 2 - 4, 25, 26 and 29

As shown in the applicant's FIGs. 4 and 7, claim 2 - 4, 25, 26 and 29 recite that the programmable delay circuit 44 (internal to jitter generator 41 of FIG. 7) resides within an IC 84. It is advantageous to embed the delay circuit in the IC being tested to prevent noise in the TEST signal that would otherwise occur if the jittery TEST signal were generated outside the IC by an IC tester, since noise makes the amount of jitter in the TEST signal unpredictable.

Claims 5 -7

Claims 5-7 recite "second means" (routing circuit 88 of FIG. 7) that can apply either the "first signal" (VIN) or the TEST signal output as an input signal to a subcircuit (85) of the IC. Routing circuit permits the jittery TEST signal to drive the subcircuit during jitter testing and permits the VIN signal to drive the subcircuit during normal IC operation.

Claims 8 and 9

Referring to FIG. 6, claims 8 and 9 recite "third means (test unit 70) residing within the IC (62) for generating the first signal

(VIN)" Thus in this version of the invention, the original test signal VIN is generated inside the IC and jitter generator 41, also inside the IC, adds jitter to it to produce the jittery TEST signal. Generating not only the TEST signal but also the VIN signal inside the IC helps to further eliminate noise in the TEST, thereby helping to reduce unpredictable jitter in the TEST signal.

Claims 10 -14

Referring to FIG. 4, claims 10-14 recite "a multiplexer (42) for receiving a second signal (VIN) and for selectively supplying either the second signal or the TEST signal as the first signal (input to B1) to the programmable delay circuit (44)". As discussed in specification paragraph 30, when multiplexer 42 feeds the TEST signal output of delay circuit 44 back to its input, the TEST signal oscillates as recited in claims 10-14 "with a period that is a function of the delay provided by the programmable delay circuit". This feature of the invention is beneficial because it enables a measurement unit 50 (FIG. 4) to measure the delay produced by each DELAY data value by counting cycles of the TEST signal occurring during a predetermined number of cycles of a stable reference clock and to report the results to an external host computer that programs and calibrates the jitter generator, by programming pattern generator 46) to produce a precise amount of jitter in the TEST signal.

Claims 15-21

Referring to FIG. 9 or 10, claims 15-21 recite that the programmable delay circuit 44 comprises "a plurality of buffers (B_1 - B_N) connected in cascade" and "a plurality of capacitive circuit elements ($L_{1,1}$ - $L_{M,N}$), each corresponding to a separate one of the buffers and each providing an adjustable capacitance at an output of its corresponding buffer, wherein the first means controls the delay … by adjusting the adjustable capacitance provided by each of the plurality of capacitive elements". This particular programmable delay circuit architecture is compact and easy to implement within an IC and permits high resolution jitter control when the DELAY data is properly calibrated.

Claims 23, 24 and 30

Claims 23, 24 and 30 and recite steps of the calibration process taught at paragraph 30 of the specification. Referring to FIG. 4, multiplexer 42 inverts the TEST signal and supplies it as input to delay circuit 44 while pattern generator 46 holds the DELAY data constant so that the TEST signal oscillates with a period that is a function of the adjustable delay (step d). Measurement unit 50 then measures the period of the TEST signal (step e). Measurement unit 50 iteratively repeats steps d and e with the adjustable delay held to different constant values during each iteration (step f). After measurement unit 50 reports the measurements to an external host computer, the host computer (as recited in claim 24) can ascertain the values of the digital control data in the DELAY data sequence needed to produce a particular jitter pattern in the TEST signal.

Claims 27 and 28

Referring to FIG. 4, claims 27 and 28 recite that the programmable delay circuit comprise "a plurality of cascade buffers (44) connected in series and means (45) for applying a capacitance of magnitude controlled by the digital delay control data (DELAY) to the outputs of the buffers."

Claims 31, 34 and 35

Specification paragraph 35 teaches that an embedded delay circuit and a programmable pattern generator can provide a jittery clock signal for use as a timing reference by a test circuit that generates signals in the IC. This causes all of signals generated inside the IC using the clock signal as a timing reference to have the same jitter. Referring to FIGs. 4 and 8, claims 31, 34 and 35 recite

"[a]n apparatus for testing a subcircuit (98) of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the apparatus comprising:

a programmable delay circuit (44) residing within the IC (84) for delaying a first clock signal (input to B1) with a delay selected by a digital delay control word input to the programmable delay circuit to produce a second clock signal (MCLK');

a programmable pattern generator (46) providing a sequence of delay control words (DELAY) as input to the programmable delay circuit;

first means (100) for selectively applying the second clock signal as the input signal to the subcircuit;

a multiplexer (42) residing within the IC for receiving a third clock signal (MCLK) and the second clock signal (MCLK') for selectively supplying either the third clock signal or the second clock signal as the first clock signal input to the programmable delay circuit, wherein the second clock signal oscillates when supplied as the first clock signal input to the programmable delay circuit with a period that is a function of the delay provided by the programmable delay circuit; and

a test circuit (96) receiving the second clock signal and for generating a test signal (TEST) having edges synchronized to edges of the second clock signal."

Claims 32 and 33

Referring to FIG. 9 or 10, claims 32 and 33 recite that the programmable delay circuit comprises "a plurality of buffers (B_1 - B_N) connected in cascade" and "a plurality of capacitive circuit elements ($L_{1,1}$ - $L_{M,N}$), each corresponding to a separate one of the buffers and each providing an adjustable capacitance at an output of its corresponding buffer, wherein the first means controls the delay … by adjusting the adjustable capacitance provided by each of the plurality of capacitive elements". This particular programmable delay circuit architecture is compact and easy to implement within an IC and permits high resolution jitter control with properly calibrated.

Grounds For Rejection To Be Reviewed On Appeal

Grounds for rejection to be reviewed on appeal are:

whether claim 1 should be rejected under 35 U.S.C. 102(b) as being anticipated by US patent 5,948,115 (Dinteman),

whether claims 2 and 3 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman and US patent 6,006,347 (Churchill),

whether claim 4 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill and U.S. patent 5,796,745 (Adams),

whether claim 5 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams and U.S. patent 5,815,512 (Osawa),

whether claim 6 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman in view of Osawa,

whether claim 7 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, Osawa and of U.S. patent 6.501.693 (Takatsuka),

whether claims 8 and 9 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, Osawa and U.S. patent 6.501.693 (Bhawmik),

whether claims 10 and 11 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman and U.S. patent 6,535,014 (Chetlur)

whether claim 12 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Chetlur and Osawa,

whether claim 13 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, Osawa, Takatsuka and Chetlur,

whether claim 14 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, Osawa, Takatsuka, Bhawmik and Chetlur,

whether claims 15, 16, 17, 18, 19, 20 and 21 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman and U.S. patent 5,144,525 (Saxe),

whether claim 22 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman and Bhawmik,

whether claims 23, 24 and 30 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Bhawmik and U.S. patent 6,611,477 (Speyer),

whether claims 25 and 29 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Bhawmik and Churchill,

whether claim 26 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, and Bhawmik,

whether claims 27 and 28 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, and Saxe,

whether claims 31, 34 and 35 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Bhawmik, Osawa, Chetlur, and Speyer

whether claims 32 and 33 should be rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Bhawmik, Osawa, Chetlur, Speyer, and Saxe

Arguments

1. Arguments against rejection of claim 1 under 35 U.S.C. 102(b) as being anticipated by Dinteman.

Claim 1

Claim 1 recites an apparatus for providing a jittery test signal comprising "a programmable delay circuit for delaying a first signal with an adjustable delay controlled by an input digital delay word to produce the jittery test signal for use in the IC." As seen in the applicant's FIGs. 4 and 6, the jittery TEST signal is used inside an IC 62 being tested. Thus regardless of whether the programmable delay circuit resides inside or outside the IC being tested, the jittery TEST signal output of the programmable delay circuit must be used inside the IC being tested.

Referring to Dinteman's FIG. 1, Dinteman teaches an IC tester external to an IC device under test (DUT) for supplying test signals to the IC and for monitoring output signals produced by the IC in response to the TEST signals. Referring to Dinteman's FIG. 4, Dinteman teaches that a tri-state buffer 42 in drive circuit 40 included a channel of an integrated circuit tester sends a TEST signal to a pin of an IC device under test in response to a DRIVE bit output of the event phase modulator 46 when enabled by an INHIBIT signal output of another event phase modulator 48. Thus the TEST signal is

used inside the IC being tested. But is this test signal produced by a programmable delay circuit as recited in claim 1?

Within modulator 46 (FIG. 6), a FIFO buffer 52 shifts in an input bit D on each pulse of a clock signal TD and shifts out an output DRIVE bit on each pulse of another clock signal TD'. A programmable delay circuit 54 delays the clock signal TD by an amount controlled DELAY data from a programmable pattern generator 56 to produce clock signal TD'. Pattern generator 56 can vary the DELAY data to vary the delay provided by delay circuit 54 so that clock signal TD' clock jitters, thereby producing jitter in the DRIVE control signal output of buffer 52 which in turn causes buffer 42 to produce jitter in the TEST signal (FIG. 4) sent to the IC provided that the INHIBIT signal input to buffer 42 is false.

The Examiner is of the opinion that the programmable delay circuit (54, FIG. 6) is "for delaying a first signal with an adjustable delay controlled by an input digital delay word to produce the jittery test signal for use in the IC" as recited in claim 1. However, the output of the programmable delay circuit 54 is not a test signal for use in the IC as recited in claim 1, but is instead a timing signal used inside and IC tester. Hence the rejection of claim 1 under 35 U.S.C. 102(b) is improper.

The Examiner (paragraph 4 of the office action dated 4/27/2006) replies to this argument by saying:

"Programmable delay circuit 54 delays the timing signal TD with a delay determined by delay data (DELAY) produced by pattern generator 56, thereby to provide a delayed timing signal TD' to a shift-out (SO) input of FIFO buffer 52".

The Examiner correctly refrains from asserting that the TD' signal is a test signal "for use in the IC" as recited in claim 1. Since the Examiner apparently agrees with the applicant's position that the output of programmable delay circuit 54 is not a test signal for use in the IC DUT but is instead a timing signal for use in clocking a FIFO buffer in an IC tester, the Examiner provides no justification for continuing to reject claim 1 in view of the applicant's argument.

2. Argument against rejection of claims 2 and 3 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman and Churchill.

Claims 2 and 3

One drawback to Dinteman's approach to supplying a jittery test signal to an IC DUT is that noise in the signal path conveying the test signal from the tester to the IC can introduce an uncontrollable amount of jitter into the test signal so that the actual jitter in the test signal arriving at the IC can vary from the controlled amount added by the tester. The applicant's claim 2 recites that the programmable delay circuit that produces the jittery test signal resides within the IC itself, so that the jittery signal is not subject to noise in a signal path conveying the test signal from the tester to the IC, as is the case for Dinteman's test signal.

Churchill (FIG. 3) teaches a test system embedded in an IC that uses a scan bus to deliver control data via a scan register 306 to a programmable delay circuit 302 within the IC which delays one test signal 314 to produce another test signal 316. The Examiner rejects claim 2 on the grounds that Churchill would motivate one of skill in the art to place Dinteman's programmable delay circuit within the IC DUT.

The applicant has argued that Churchill does not teach or suggest that his embedded programmable delay circuit should be used to produce a "jittery" test signal as recited in claim 1. The Examiner, at paragraph 5 of the office action dated 4/27/2006 makes only the following statement in response to the applicant's argument:

"The examiner disagrees and would like to mention that Dinteman teaches programmable delay circuit (fig. 6, Dinteman). Churchill only teaches that a programmable delay circuit can be within the IC (fig. 3, col. 20, lines 38-31, Churchill et al.)"

The Examiner is correct; the only relevant teaching of Churchill (which has nothing to do with jitter testing) is that that a programmable delay circuit can be within an IC, and not that such a

programmable delay circuit should be used to create a jittery test signal for use within the IC as recited in claims 2 and 3.

The applicant concedes that is well-known to implement programmable delay circuits within ICs for various purposes, however it one were to implement Dinteman's programmable delay circuit 54 of FIG. 6 inside the IC DUT, then the TD clock signal input to the delay circuit would have to be sent to the DUT from the IC tester in order to be delayed by the delay circuit, the delayed TD' clock signal output of the programmable delay circuit would have to return to the IC DUT in order to clock the SO terminal of FIFO buffer 52 so that its DRIVE signal output could drive tristate buffer 42 of FIG. 4 to produce the TEST signal, which would then have to be sent to the ID DUT. Thus moving Dinteman's programmable delay circuit 54 into the IC DUT, as the Examiner suggests, would increase the number of connections between the IC tester and the IC DUT from one (the TEST signal) to three (the TD signal, the TD' signal and the TEST signal). This would not only require the IC to have two additional terminals for each IC input terminal (if all IC input signals were to be subjected to jitter testing), it would also increase the noise in the TEST signal supplied to each IC input terminal. Thus one of skill in the art would not be motivated to move Dinteman's programmable delay circuit into the IC simply by the knowledge that programmable delay circuits can be implemented within ICs.

If one were to move all of Dinteman's event phase modulator 46 of FIG. 4 (including pattern generator 56, programmable delay circuit 54, and FIFO buffer 52 (FIG. 6) as well as tristate buffer 42 into the IC DUT, separate DRIVE and INHIBIT signals of FIG. 4 would have to be sent to the DUT for each IC input signal, thereby doubling the number of IC input terminals, which would be an improvement over the result of the Examiner's approach of moving only the programmable delay circuit into the IC, but still hardly an improvement over Dinteman's original approach, and hardly something one of skill in the art would consider doing.

The applicant has also argued that Dinteman would not motivate one of skill in the art to use Churchill's system to produce a jittery test signal because it would not be possible to do so. To produce a controlled amount of jitter in the output signal 316 of Churchill's

programmable delay circuit 302 (FIG. 3) as taught by the applicant, it would be necessary to supply control data to programmable delay circuit 302 that changes at the rate at which state changes in the test signal occur because it is necessary to independently control the timing of each edge of signal 316. Thus data would have to be written into scan register 306 at the clock rate of the input signal to delay circuit 316. An external host computer serially shifts the data into Churchill's scan register 306 via a scan bus. A scan bus is typically used during testing to shift data in and out of registers within an IC, for example to reset or check the states of various signals within the IC, but not when the IC is actively processing input signals at its rated clock frequency, as would be the case during a jitter test. Changing the data in a scan register requires many clock cycles. To do so, an IC test is halted, data is shifted in and out of the IC via the scan bus to read the contents of write data into all scan registers, and the test is then resumed. Dinteman would not therefore motivate one of skill in the art to use Churchill's programmable delay circuit 302 to produce a jittery test signal for use in jitter testing because the scan bus could not supply data to frequency modulate input signal 314 at a sufficient rate during a jitter test in which the IC is supposed to be responding to a jittery test signal.

Thus claim 2, and its dependant claim 3, are patentable over the combination of Dinteman and Churchill.

3. Argument against rejection of claim 4 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill and Adams.

Claim 4

Claim 4 depends on claim 3 and recites "the first means (the programmable pattern generator) resides within the IC." Combining the teaching of three patents to reject claim 4, the Examiner cites Dinteman and Churchill as teaching the underlying subject matter of claim 3 and cites Adams only as teaching that a programmable pattern generator can be embedded in an IC. Claim 4 is patentable over the combination of Dinteman and Churchill and Adams because, as discussed

above Dinteman and Churchill fail to teach limitations of parent claim 3 and also because Adams fails to motivate one of skill in the art to move Dinteman's pattern generator into the IC DUT.

Adams teaches a built-in self, test (BIST) circuit within an IC including a pattern generator for supplying its output data as data, address and control signal inputs to a memory under test, rather than to a delay circuit. Adam's BIST circuit does not perform jitter testing. The Examiner suggests that Adams would motivate one of skill in the art to embed Dinteman's pattern generator 56 in the IC being tested rather than place it in the IC tester as taught by Dinteman. Note, however, that Dinteman's pattern generator 56 (FIG. 6) supplies control data (DELAY) to a delay circuit 54 inside the tester that produces not a jittery test signal for use inside an IC, but a timing signal TD' used to control a FIFO buffer inside the tester. As discussed above, one of skill in the art would not be motivated to move any subset of the portion of Dinteman's IC tester that creates a jittery test signal (including pattern generator, programmable delay circuit FIFO buffer, and tristate buffer) into the IC DUT because doing so would require additional IC pins, would increase the noise in the TEST signal, and would provide no benefit.

The Examiner, at paragraph 6 of the office action dated 4/27/2006 makes only the following statement to rebut the applicant's arguments with respect to claim 4:

"The Examiner disagrees and would like to point out that Adams et al teaches an ABIST circuit on an integrated circuit including a programmable pattern generator (fig. 1, col. 3, lines 31-33, Adams et al.)

The applicant's concedes that including a programmable pattern generator in a BIST circuit is well-known, however Adam's BIST circuit has nothing to do with jitter testing, and the Examiner's statement does not address the issues raised by the applicant's argument.

4. Argument against rejection of claim 5 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams and Osawa.

Claim 5

Claim 5 depends on claim 4, and the Examiner cites Osawa as teaching only the additional limitations of claim 4. Claim 5 is therefore patentable over the combination of Dinteman, Churchill, Adams and Osawa because Dinteman, Churchill, and Adams fail to teach limitations of claim 4 as discussed above. Claim 5 is further patentable over the cited references because Osawa fails to teach the additional limitations of claim 5.

Claim 5 recites "the IC includes a subcircuit" and that the apparatus further comprises "second means within the IC for selectively applying either the first signal or the test signal as an input signal to the subcircuit." As discussed in specification paragraph 30, this refers to multiplexer 42 of the applicant's FIG. 4 which can feed the TEST signal back to the delay circuit input during calibration to cause the TEST signal to oscillate, thereby allowing measurement unit 50 to measure the period of the TEST signal to determine the delay through the delay circuit for a given DELAY data setting.

The Examiner points to Osawa (FIG. 1) as showing a multiplexer 233 included in a scan register to select between a data signal output D of a semiconductor device and a serial signal SI from an external source. The applicant has argued that Osawa provides no motivation for one of skill in the art to use Osawa's selector in connection with Dinteman's jitter generator circuit because Osawa's circuit has nothing to do with jitter testing, and because Osawa's multiplexer does not select between the input to a programmable delay circuit and the output of the programmable delay circuit as recited in the applicant's claim 5. The Examiner, at paragraph 7 of the office action dated 4/27/2006 makes the following statement in reply the applicant's arguments with respect to claim 5:

"Dinteman teaches that in decoding the incoming VECTOR, decoder 62 signals a set of four multiplexers 76 (fig. 8, col. 7, lines 28-29, Dinteman). Osawa et al teaches selector circuit 233 (fig. 1, col. 2, lines 57-67, Osawa et al.). Thus Dinteman provides motivation to use Osawa's selector in connection with Dinteman's jitter generator circuit."

Apparently the Examiner's position is that since both Dinteman and Osawa disclose the existence of multiplexers used for purposes other than as recited in claim 5, one of skill in the art would find it obvious to use a multiplexer for the purpose recited in claim 5, selectively connecting the output of a delay circuit in an embedded jitter generator to its input so that its output signal oscillates. The Examiner's understanding of obviousness is in error. Almost all patentable inventions are combinations of known elements, but the mere existence of elements of the invention in prior art applications is not considered sufficient motivation for one of skill in the art to combine them as recited in a claim. The Examiner must show that the prior art teaches to combine such elements in the manner claimed.

5. Argument against rejection of claim 6 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman in view of Osawa.

Claim 6

Since claim 6 depends on claim 5, rather than on claim 1, the applicant assumes the Examiner intended to reject claim 6 as unpatentable over the combination of Dinteman, Churchill, Adams and Osawa rather than over the combination of only Dinteman and Osawa. Claim 6 is patentable over the combination of Dinteman, Churchill, Adams and Osawa for reasons discussed above in connection with its parent claim 5.

6. Argument against rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, Osawa and Takatsuka.

Claim 7

Claim 7 depends on claim 6 and the Examiner cites Takatsuka as teaching only the additional limitations of claim 7, since Takatsuka does not relate to a jitter testing circuit. Claim 7 is therefore patentable over the combination of Dinteman, Churchill, Adams, Osawa

and Takatsuka because Dinteman, Churchill, Adams and Osawa fail to teach the underlying limitations of claim 6 as discussed above.

<u>7. Argument against rejection of claims 8 and 9 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, Osawa and Bhawmik.</u>

Claims 8 and 9

Claim 8 depends on claim 7, and the Examiner cites Bhawmik as teaching only the additional limitations of claim 7. Claim 8 is therefore patentable over the combination of Dinteman, Churchill, Adams, Osawa, and Bhawmik because Dinteman, Churchill, Adams and Osawa fail to teach limitations of claim 7 as discussed above. Claim 8 is further patentable over the cited references because Osawa fails to teach the additional limitations of claim 8.

Claim 8 recites that the apparatus further comprises "third means residing within the IC for generating the first signal." which is supported by test unit 70 of the applicant's FIG. 6. Thus claim 8 implies that the "first signal" that is variably delayed to produce the test signal is also generated within the IC.

The Examiner cites Bhawmik (col. 1, lines 16-23) as teaching generating test signals inside an IC, perhaps suggesting that Bhawmik motivates one to move a separate copy of Dinteman's <u>entire</u> integrated circuit tester channel inside the IC DUT for each input signal of the IC that is to be subject to jitter testing. However in addition to the obvious IC floor space limitations that would prevent one from doing so, implementing Dinteman's tester channels as BIST circuits within the IC DUT being tested would not produce a result that is equivalent to the apparatus of claim 8 for reasons expressed above in connection with claim 1. Note also that nothing in Bhawmik relates to jitter testing or otherwise indicates that Bhawmik's internally generated test signal can or should be applied as input to a programmable delay circuit within the IC which adds a controlled amount of jitter to the test signal.

The Examiner, at paragraph 9 of the office action dated 4/27/2006 makes the following statement in reply to the applicant's arguments against rejection of claim 8:

"Dinteman teaches input to a programmable delay circuit within the IC, which adds a controlled amount of jitter to the signal [and] Bhawmik et al. teach a third means residing with the IC for generating the first signal …."

It is clear, however that Dinteman's programmable delay circuit 56 of FIG. 6 resides in a tester that is external to the IC DUT being tested and is not within the IC DUT as the Examiner states. In any case in order to make Dinteman's jitter circuit meet the limitations of claim 8 it would be necessary to do the following:

1. move Dinteman's jitter circuit of FIG. 6 into Bhamik's IC,
2. modify Dinteman's jitter circuit to eliminate the FIFO buffer,
3. further modify Dinteman's jitter circuit to obtain the input to Dinteman's programmable delay circuit from Bhamik's embedded test circuit rather than from a clock source in an IC tester,
4. further modify Dinteman's jitter testing circuit to use the output of the programmable delay circuit rather than the output of the FIFO buffer as the jittery test signal,
5. further modify Dinteman's jitter circuit to provide selective feedback of its output test signal to its input (as recited in a parent claim 5 of claims 8 and 9),
6. further modify Dinteman's jitter circuit to obtain a source for clock signal TD inside the IC that is synchronous with the output of Bhamik's test circuit, and
7. further modify Dinteman's jitter circuit to provide alternate input signal sources to the IC subcircuit (as recited in parent claim 7).

Despite the need to make such a large number of modifications to Dinteman's jitter circuit in order to get it to meet the limitations of claim 8, the Examiner considers the applicant's claim 8 to be obvious in view of the combination of Dinteman and five other patents, none of which relate to jitter testing, and which at best disclose only the use of bits and pieces of the applicant's invention in

contexts that do not relate to jitter testing. The Examiner fails to provide any compelling reason why any of these six references would motivate one to so extensively modify Dinteman's jitter circuit.

Claim 9 is patentable over the cited references for reasons similar to those discussed above in connection with claim 8.

8. Argument against rejection of claims 10 and 11 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman and Chetlur.

Claim 10

Claim 10 depends on claim 1, and the Examiner cites Chetlur as teaching only the additional limitations of claim 1. Claim 10 is therefore patentable over the combination of Dinteman and Chetlur because Dinteman fails to teach limitations of claim 1 as discussed above. Claim 10 is further patentable over the cited references because Chetlur fails to teach the additional limitations of claim 10.

Claim 10 recites a multiplexer that can feed the test signal output of the programmable delay circuit back to the input of the programmable delay circuit so that the test signal oscillates. See the applicant's FIG. 4. As discussed above, this allows the programmable delay circuit to generate an oscillating test signal for calibration purposes without deriving it from the IC input signal VIN.

The Examiner correctly points out that Dinteman does not disclose such a multiplexer that allows the output signal TD' of Dinteman's programmable delay circuit 54 of FIG. 6 to be fed back to its input. The Examiner points to Dinteman (col. 5, lines 45-46, col. 6, lines 16-20, col. 6, lines 30-34) as teaching a test signal that oscillates with a period that is a function of the delay provided by the programmable delay circuit when the test signal output of the programmable delay circuit is fed back to the delay circuit's inputs. However col. 5, lines 45-46 teach only that the delay of a programmable delay circuit is specified by its input data. Lines 16-20 of col. 6 teach that when the delay of the programmable delay circuit is fixed, the DRIVE signal output of buffer 52 (FIG. 6) looks like its D signal input, and col. 6, lines 30-34 simply describe the architecture of Dinteman's FIG. 4. Nothing in any of the cited

sections of Dinteman mention anything about any signal output of a delay circuit that can be fed back to the delay circuit's input so that the signal oscillates with a period that is a function of the delay of the delay circuit as recited in claim 10.

The Examiner cites Chetlur (FIG. 1) as teaching a selector 14 that receives a test signal from a multiplexer 13 and a second signal VG to produce an input signal VIN to a "circuit path" 11, but selector 14 does not selectively apply the test signal <u>output</u> of a programmable delay circuit to the delay circuit's <u>input</u> to cause the VIN signal to oscillate.

The Examiner, at paragraph 9 of the office action dated 4/27/2006, replies to the applicant's arguments by stating:

"Chetlur et al. teach a tester comprising a voltage controlled oscillator for generating a controllable frequency oscillating test signal (col. 6, lines 14-15, Chetlur et al.). Chetlur et al. also teach that the multiplier supplies the test signal as the first signal input (fig. 1, col. 6, lines 22024, Chetlur et al.)."

While VCO 12 of Chetlur's FIG. 1 may include an internal delay circuit, it does not appear to be programmable, and neither selector 14 or multiplexer 13 selectively apply a test signal <u>output</u> of any programmable delay circuit (whether inside VCO 12 or not) back to its <u>input</u> as does the multiplexer of the applicant's claim 10.

Claim 11

Claim 11 depends on claim 10 and is patentable over the cited references for similar reasons. Claim 11 further recites "third means for generating data that is a function of a period of the test signal when the multiplexer supplies the test signal as the first signal input to the programmable delay circuit". The third means is supported by the applicant's measurement unit 50 of FIG. 4. As discussed above, neither Dinteman nor Chetlur teach a multiplexer that feeds a test signal output of a programmable delay circuit back to the delay circuit's input.

The Examiner cites Dinteman (FIGs. 2 and 6, col. 2, lines 3-38 and col. 6, lines 39-43) as teaching a device for generating data that

is a function of the TEST signal. FIG. 6 shows no device for generating data that is a function of a period of any oscillating test signal supplied to an IC. FIG. 2 shows a compare circuit 28 that generates data that is a function of the output (DUT_OUT) of an IC device under test (DUT). Since the DUT_OUT signal can arrive at the tester on the same bi-directional line that may be used to send a TEST signal to the DUT, the TEST signal may appear to be an input to compare circuit 28, but the compare circuit does not generate output FAIL data that is "a function of the <u>period</u> of the test signal as recited in claim 11" even if the compare circuit were used to monitor the TEST signal instead of the DUT_OUT signal. The Examiner cites Dinteman (col. 2, lines 3-38 and col. 6, lines 39-43) as teaching this, but these sections of Dinteman teach nothing about any device that generates data that is a function of the period of a test signal output of an oscillator produced by feeding back the test signal to the input of the oscillator.

The Examiner, at paragraph 9 of the office action dated 4/27/2006, replies to the applicant's arguments by stating:

"Dinteman teach a delay circuit (fig. 6, Dinteman). Dinteman also teaches a driver circuit 40 can produce a TEST signal that is a phase modulated version of the TEST signal defined by the input VECTOR data sequence, with the nature of the phase modulating being determined by the programming data input to event phase modules 46 and 48 (col.5, lines 51-56, Dinteman)."

The Examiner's observation is entirely correct, but completely irrelevant to the applicant's arguments against rejection of claim 11. The additional limitations of claim 11 do not involve an apparatus involving two event phase modules, a tri-state driver circuit, and a VECTOR data sequence that defines a TEST signal.

<u>9. Argument against rejection of claim 12 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Chetlur and Osawa.</u>

Claim 12

The Examiner incorrectly relies on Dinteman as teaching the underlying subject matter of parent claim 1 of claim 12 for reasons discussed above in connection with claim 1.

The Examiner incorrectly relies on Chetlur as teaching the multiplexer recited in claim 12, for reasons discussed above in connection with claims 10 and 11.

The Examiner incorrectly relies Osawa as teaching the recited "second means" of claim 12 for reasons discussed above in connection with claim 5.

10. Argument against rejection of claim 13 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, Osawa, Takatsuka and Chetlur.

Claim 13

The Examiner incorrectly relies on the combination of Dinteman, Chetlur and Osawa as teaching the underlying subject matter of parent claim 12 of claim 13 as discussed above in connection with claim 12.

The Examiner incorrectly relies on the combination of Churchill, Adams and Takatsuka as teaching additional limitations of claim 13 regarding the recited "first means", "second means" and "multiplexer" for reasons discussed in the applicant's arguments above in connection with claims 2, 4 and 7.

11. Argument against rejection of claim 14 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, Osawa, Takatsuka, Bhawmik and Chetlur.

Claim 14

The Examiner incorrectly relies on the combination of Dinteman, Churchill, Adams, Osawa, Takatsuka, Bhawmik and Chetlur as teaching the underlying subject matter of the parent claim 13 of claim 14 as discussed above in connection with claim 13.

Claim 14 further recites "third means residing within the IC for generating data that is a function of a period of the test signal when test signal oscillates." The Examiner incorrectly relies on Bhawmik

as teaching the recited "third means" as discussed in the applicant's arguments above in connection claims 8 and 9.

12. Argument against rejection of claims 15, 16, 17, 18, 19, 20 and 21 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman and Saxe.

Claims 15-21

The Examiner cites Dinteman as teaching the underlying subject matter of claim 1 and cites Saxe as teaching the additional limitations of claims 15-21. Claims 15-21 are patentable over the combination of Dinteman and Saxe because, as discussed above relative to claim 1, Dinteman fails to teach limitations of claim 1. The Examiner cites Saxe only as teaching the additional limitations of claims 15-21. Claims 15-21 are therefore patentable over the cited references.

13. Argument against rejection of claim 22 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman and Bhawmik.

Claim 22

Claim 22 recites that a test signal supplied as input to a subcircuit of an IC being tested is produced at the output of a programmable delay circuit which variably delays a first signal so that the test signal jitters. The Examiner cites Dinteman as teaching this, however the output signal TD' of Dinteman's programmable delay circuit of FIG. 6 is not a test signal but is instead a timing signal for use only within an IC tester for controlling the shift out terminal of FIFO buffer 52.

The Examiner cites Bhawmik only as teaching to apply a test signal to a subcircuit of an IC under test. Bhawmik would not motivate one of skill in the art to supply the timing signal output TD' of the Dinteman's programmable delay circuit 54 as input to a subcircuit of an IC under test since Dinteman's timing signal TD' is not a test signal intended for that purpose.

The Examiner (paragraph 13 of the office action dated 4/27/2006) replies to the applicant's argument by saying:

"Programmable delay circuit 54 delays the timing signal TD with a delay determined by delay data (DELAY) produced by pattern generator 56, thereby to provide a delayed timing signal TD' to a shift-out (SO) input of FIFO buffer 52".

The Examiner correctly identifies the output signal TD' of the programmable pattern generator 56 as a timing signal used to control a device in a tester rather than a test signal as recited in claim 1. However, the Examiner's comments support rather than refute the applicant's arguments against rejection.

14. Argument against rejection of claims 23, 24 and 30 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Bhawmik and Speyer.

Claim 23, 24 and 30

The Examiner cites Dinteman and Bhawmik as teaching the underlying subject matter of parent claim 22 and cites Speyer only as teaching the additional limitations of its dependant claims 23, 24 and 30. Claims 23, 24 and 30 are patentable over the combination of Dinteman Bhawmik and Speyer because, as discussed above relative to claim 22, Dinteman and Bhawmik fail to teach the additional limitations of parent claim 22.

As discussed in specification paragraph 30, claims 23, 24 and 30 recites applying the test signal as input to the programmable delay circuit (step d) so that the test signal oscillates, measuring the period of the test signal (step e) and carrying out a plurality of iterations of steps d and e with the adjustable delay held to a different constant value during each iteration.

Speyer (FIG. 2) shows a BIST circuit for measuring a delay through a test circuit 205 by comparing counts of cycles of the output 265 of a ring oscillator when the test circuit 205 is included in as an element of the ring oscillator and when it is not. Switch 270 selectively includes/excludes the test circuit in/from the ring. The

Examiner cites Speyer as teaching an oscillator that includes a delay circuit formed by feeding the circuit back to its input and suggests one of skill in the art would be motivated to somehow modify Dinteman's circuit of FIG. 6 as taught by Speyer because doing so "would provide an oscillating test signal".

However turning Dinteman's programmable delay circuit 54 into an oscillator and using its output as an oscillating test signal input to the IC DUT would decouple the timing of the TD' signal from the timing of other channels within the IC tester which are also synchronized to the TD signal, thereby causing the tester channel to loose synchronicity with the other tester channels. One of skill in the art would not be motivated to do that since it is well-known that all tester channels must be closely synchronized in order to properly test an IC.

The Examiner (paragraph 14 of the office action dated 4/27/2006) replies to this argument saying:

"The examiner disagrees and contends that Speyer et al. teach phase discriminator 215 and test circuit 205 function as a ring oscillator in which the period of oscillation is determined by the signal propagation delay (col. 4, line 42045, Speyer et al). Dinteman teaches a programmable delay circuit (fig. 6, Dinteman).

Thus the Examiner is apparently of the opinion that since Speyer teaches a step of including a delay circuit in a ring oscillator in an application (measuring a delay through a test circuit) that has nothing to do with Dinteman's application (generating a jittery test signal) and nothing to do with the applicant's reason for connecting a delay circuit's output to its input (calibration of a jitter generator circuit), then one of skill in the art would be motivated to turn Dinteman's delay circuit into a ring oscillator. The Examiner's opinion as to the motivation provided by Speyer is incorrect.

15. Argument against rejection of claims 25 and 29 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Bhawmik and Churchill.

Claims 25 and 29

The Examiner cites Dinteman and Bhawmik as teaching the underlying subject matter of claim 22 and cites Churchill as teaching the additional limitations of claims 25 and 29. Claims 25 and 29 are patentable over the combination of Dinteman, Bhawmik and Churchill because, as discussed above relative to claim 22, Dinteman and Bhawmik fail to teach limitations of claim 22.

The Examiner points to Churchill (Fig. 3) as teaching to form the programmable delay circuit 302 in the IC being tested as recited in claims 25 and 29. However as discussed above in connection with claim 3, one of skill in the art would not be motivated to use Churchill's programmable delay circuit 302 to produce a jittery test signal because it is controlled by data supplied by a scan bus that could not supply data to frequency modulate input signal 314 at a sufficient rate when the IC is processing the test signal 316. Also, as discussed above in connection with claim 3, since Dinteman's programmable delay circuit produces a timing signal used to control a circuit within the tester rather than a test signal supplied to the IC under test, one of skill in the art would not be motivated to embed the programmable pattern generator that supplied state to the delay circuit in the IC. Thus Churchill would not motivate one of skill in the art to embed Dinteman's programmable delay circuit in the IC being tested.

16. Argument against rejection of claim 26 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, and Bhawmik.

Claim 26

The Examiner cites Dinteman, Churchill and Bhawmik as teaching the underlying subject matter of claim 25 and cites Adams as teaching the additional limitations of claim 26. Claim 26 is patentable over the combination of Dinteman, Churchill, Adams, and Bhawmik because, as discussed above relative to claim 25, Dinteman, Churchill and Bhawmik fail to teach limitations of claim 25.

The Examiner points to Adams as teaching a pattern generator embedded in an IC as recited by claim 26 and suggests that Adams would

motivate one of skill in the art to embed the pattern generator 56 of Dinteman in the IC being tested rather than place it in the IC tester. However note that Dinteman's pattern generator 56 (FIG. 6) supplies control data (DELAY) to a delay circuit 54 inside the tester that produces a timing signal TD' also used inside the tester. Pattern generator 56 does not supply control data to a delay circuit inside the IC DUT and which produces a test signal used <u>inside the IC</u>. The DELAY data and the TD' signal it controls are needed <u>inside the tester</u> because the TD' signal is a timing signal needed to control a part in the tester and is not a test signal supplied to the CI under test. Thus one of skill in the art would not be motivated to embed pattern generator 56 in the IC under test since it would render Dinteman's test circuit non-functional.

17. Argument against rejection of claims 27 and 28 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Adams, and Saxe.

Claims 27 and 28

The Examiner cites Dinteman, Churchill and Bhawmik as teaching the underlying subject matter of claim 25 and cites Saxe as teaching the additional limitations of claims 27 and 28. Claims 27 and 28 are patentable over the combination of Dinteman, Bhawmik, Churchill and Saxe because, as discussed above relative to claim 25, Dinteman, Churchill and Bhawmik fail to teach limitations of claim 25. The Examiner cites Saxe only as teaching the additional limitations of claims 27 and 28. Claims 27 and 28 are therefore patentable over the cited references.

18. Argument against rejection of claims 31, 34 and 35 under 35 U.S.C. 103(a) as being unpatentable over the combination of Dinteman, Churchill, Bhawmik, Osawa, Chetlur, and Speyer.

Claims 31, 34 and 35

Relative to claims 31, 34 and 35, the Examiner cites Churchill as motivating one of skill in the art to place Dinteman's programmable delay circuit within the IC being tested. As mentioned above, in

order to produce jitter in a test signal (such as Churchill's signal 316) it would be necessary to supply control data to programmable delay circuit 302 that changes at the rate at which state changes in the test signal occur because it is necessary to independently control the timing of each edge of the test signal. One of skill in the art would not be motivated to use Churchill's embedded programmable delay circuit 302 to produce a jittery test signal because the scan bus could not supply data to frequency modulate input signal 314 at a sufficient rate during an at-speed test when the IC is processing the test signal 316.

The Examiner cites Osawa (FIG. 1) as showing a selector circuit 233 that can selectively supply either of its two input signals as an output signal. Osawa's selector 233 is included in a scan register to select between a data signal output D of a semiconductor device and a serial signal SI from another source. Osawa's circuit has nothing to do with jitter testing and does not select between the <u>input</u> to a programmable delay circuit and the jittery <u>output</u> of the programmable delay circuit as recited in the applicant's claim 5. Thus Osawa provides no motivation for one of skill in the art to use Osawa's selector as the recited "first means" in connection with Dinteman's jitter generator circuit.

The Examiner cites Chetlur (FIG. 1) as teaching a selector 12 that receives a test signal from a multiplexer 14 and a second signal VG to produce an input signal VIN to a "circuit path", but the selector 12 does not feed back the test signal output of a programmable delay circuit to the delay circuit's input to cause the test signal to oscillate and therefore does not suggest the "multiplexer" recited in claims 31, 34 and 35.

The Examiner cites Speyer as teaching an oscillator formed by feeding the output of a delay circuit back to its input, and suggests that one of skill in the art would be motivated to modify Dinteman's circuit in this manner because doing so would provide an oscillating test signal. However since the output of Dinteman's programmable delay circuit is a timing signal TD' and not a test signal, one of skill in the art would not be motivated to modify Dinteman's test circuit in such manner. It would also decouple the timing of the TD' signal from the timing of other circuits within the IC tester which

are synchronized to the TD signal, thereby causing the tester channel to lose synchronicity with the other tester channels. One of skill in the art would not consider doing that.

19. Argument against rejection of claims 32 and 33 as being unpatentable over the combination of Dinteman, Churchill, Bhawmik, Osawa, Chetlur, Speyer, and Saxe.

Claims 32 and 33

The Examiner cites Dinteman, Bhawmik, Osawa, Chetlur, Churchill, and Speyer as teaching the underlying subject matter of claim 31. Claims 32 and 33 are patentable over the combination of Dinteman, Bhawmik, Osawa, Chetlur, Churchill, Speyer and Saxe because, as discussed above relative to claim 31, Dinteman, Bhawmik, Osawa, Chetlur, Churchill, and Speyer fail to teach limitations of claim 31. The Examiner cites Saxe only as teaching the additional limitations of claims 32 and 33.

Claims Appendix

1. An apparatus for providing a jittery test signal for use in an integrated circuit (IC) test, the apparatus comprising:

a programmable delay circuit for delaying a first signal with an adjustable delay controlled by an input digital delay word to produce the jittery test signal for use in the IC, and

first means for supplying a sequence of digital data words as input to the programmable delay circuit for varying the adjustable delay so that the test signal jitters relative to the first signal.

2. The apparatus in accordance with claim 1 wherein the programmable delay circuit resides within the IC.

3. The apparatus in accordance with claim 2 wherein the first means comprises a programmable pattern generator.

4. The apparatus in accordance with claim 3 wherein the first means resides within the IC.

5. The apparatus in accordance with claim 4 wherein the IC includes a subcircuit and wherein the apparatus further comprises:

second means within the IC for selectively applying either the first signal or the test signal as an input signal to the subcircuit.

6. The apparatus in accordance with claim 5 further comprising:

means for delivering the first signal from an input terminal of the IC to the second means.

7. The apparatus in accordance with claim 5 further comprising:

second means within the IC for selectively applying either a second signal or the test signal as an input signal to the subcircuit.

8. The apparatus in accordance with claim 7 further comprising:

third means residing within the IC for generating the first signal.

9. The apparatus in accordance with claim 8 wherein the third means also monitors an output signal of the subcircuit to determine whether it behaves in a particular manner while the second means applies the test signal as the input signal to the subcircuit.

10. The apparatus in accordance with claim 1

wherein the first means alternatively continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant, and

wherein the apparatus further comprises:

a multiplexer for receiving a second signal and the test signal and for selectively supplying either the second signal or the test signal as the first signal input to the programmable delay circuit, wherein the test signal oscillates when the multiplexer supplies the test signal as the first signal input to the programmable delay circuit with a period that is a function of the delay provided by the programmable delay circuit when the first means continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant.

11. The apparatus in accordance with claim 10 further comprising:

third means for generating data that is a function of a period of the test signal when the multiplexer supplies the test signal as the first signal input to the programmable delay circuit while the first means continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant.

12. The apparatus in accordance with claim 1

wherein the first means comprises a programmable pattern generator for supplying a sequence of digital delay data words to the programmable delay circuit for varying its delay with time and for alternatively continuously supplying a digital data word to the programmable delay circuit to hold its delay constant,

wherein the IC includes a subcircuit, and

wherein the apparatus further comprises:

second means for selectively applying the test signal as an input signal to the subcircuit; and

a multiplexer for receiving a second signal and the test signal and for supplying the second signal as the first signal input to the programmable delay circuit while the first means is supplying the sequence of digital delay words to the programmable delay circuit and for supplying the test signal as the first signal input to the programmable delay circuit while the first means is continuously supplying a digital data word to the programmable delay circuit to hold its delay constant,

wherein the test signal oscillates when the multiplexer supplies the test signal as the first signal input to the programmable delay circuit with a period that is a function of the constant delay of the programmable delay circuit.

13. The apparatus in accordance with claim 12 wherein the programmable delay circuit, the programmable pattern generator, the second means, and the multiplexer reside within the IC.

14. The apparatus in accordance with claim 13 further comprising:

third means residing within the IC for generating data that is a function of a period of the test signal when test signal oscillates.

15. The apparatus in accordance with claim 1 wherein the programmable delay circuit comprises:

a plurality of buffers connected in cascade, each having an output; and

a plurality of capacitive circuit elements, each corresponding to a separate one of the buffers and each providing an adjustable capacitance at an output of its corresponding buffer, wherein the first means controls the delay of the programmable delay circuit by adjusting the adjustable capacitance provided by each of the plurality of capacitive elements.

16. The apparatus in accordance with claim 15 wherein first means always adjusts the adjustable capacitance of the capacitive

circuit elements so that they provide substantially similar amounts of capacitance at the outputs of their corresponding buffers.

17. The apparatus in accordance with claim 15 wherein first means independently adjusts the adjustable capacitance of each capacitive circuit element.

18. The apparatus in accordance with claim 15 wherein first means can adjust the adjustable capacitance of at least two of the capacitive circuit elements so that they provide differing amounts of capacitance at the outputs of their corresponding buffers.

19. The apparatus in accordance with claim 15 wherein each capacitive circuit element comprises:

a plurality of capacitors, and

a plurality of switches controlled by the first means for coupling selected ones of the capacitors to the output of the buffer corresponding to the capacitive circuit element.

20. The apparatus in accordance with claim 19 wherein each capacitor is provided by an input of a gate having capacitive input impedance.

21. The apparatus in accordance with claim 15 wherein each capacitive circuit element comprises:

a plurality of gates having inputs linked to the output of the buffer corresponding to the capacitive circuit element, wherein an input capacitance of each gate is a function of a voltage applied to the gate, wherein the first means controls a magnitude of the voltage applied to each gate.

22. A method for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the method comprising the steps of:

a. providing a programmable delay circuit having an adjustable delay controlled by digital delay control data supplied to the programmable delay control circuit;

b. applying a first signal as input to the programmable delay circuit such that the programmable delay circuit delays the first signal to produce a test signal, and

c. supplying a sequence of digital control data to the programmable delay circuit that varies the adjustable delay during step b such that the test signal jitters relative to the first signal.

23. The method in accordance with claim 22 further comprising the steps of:

d. inverting and applying the test signal as input to the programmable delay circuit and supplying digital delay control data to the programmable delay circuit that holds its adjustable delay constant, such that the test signal oscillates with a period that is a function of the adjustable delay;

e. measuring the period of the test signal;

f. carrying out a plurality of iterations of steps d and e with the adjustable delay held to a different constant value during each iteration.

24. The method in accordance with claim 22 further comprising the step of:

g. ascertaining values of digital control data included in the sequence supplied at step c needed to produce a particular jitter pattern in the test signal generated at step c based on the periods of the test signal measured during the plurality of iterations of step e.

25. The method in accordance with claim 22 wherein step a comprises the forming the programmable delay circuit within the IC.

26. The method in accordance with claim 25 wherein step c comprises the substeps of:

c1. forming a programmable pattern generator within the IC; and

c2. programming the programmable pattern generator to generate the sequence of digital delay control data.

27. The method in accordance with claim 25 wherein the programmable delay circuit comprises:

a plurality of cascaded buffers connected in series, each having an output; and

means for applying a capacitance of magnitude controlled by the digital delay control data to the outputs of the buffers.

28. The method in accordance with claim 27 wherein any change in value of the digital delay control data applied to the programmable delay circuit during step c causes a change in the magnitude of the capacitance applied to the output of each of the cascaded buffers.

29. The method in accordance with claim 25 further comprising the step of:

d. providing means within the IC for monitoring the output signal of the subcircuit to determine whether the output signal behaves in a particular manner and for sending data from the IC indicating wherein the output signal behaved in that particular manner.

30. The method on accordance with claim 23 wherein step e comprises counting a number of periods of a periodic reference clock signal occurring during a predetermined number of periods of the test signal.

31. An apparatus for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal, the apparatus comprising:

a programmable delay circuit residing within the IC for delaying a first clock signal with a delay selected by a digital delay control word input to the programmable delay circuit to produce a second clock signal;

a programmable pattern generator for providing a sequence of delay control words as input to the programmable delay circuit;

first means for selectively applying the second clock signal as the input signal to the subcircuit;

a multiplexer residing within the IC for receiving a third clock signal and the second clock signal for selectively supplying either the third clock signal or the second clock signal as the first clock signal input to the programmable delay circuit, wherein the second clock signal oscillates when supplied as the first clock signal input to the programmable delay circuit with a period that is a function of the delay provided by the programmable delay circuit; and

a test circuit receiving the second clock signal and for generating a test signal having edges synchronized to edges of the second clock signal.

32. The apparatus in accordance with claim 31 wherein the programmable delay circuit comprises:

a plurality of buffers connected in series, each having an output; and

second means for adding capacitance of magnitude controlled by each successive digital delay control word of the sequence to outputs of the buffers.

33. The apparatus in accordance with claim 32 wherein the second means comprises:

a plurality of capacitors, and

a plurality of switches controlled by each successive delay control word of the sequence for selectively coupling the capacitors to inputs of the buffers.

34. The apparatus in accordance with claim 31 further comprising:

second means residing within the IC for monitoring the output signal of the subcircuit to determine whether it behaves in a particular manner in response to the test signal.

35. The apparatus in accordance with claim 31 further comprising:

second means for counting a number of periods of a periodic reference clock signal occurring during a predetermined number of periods of the test signal.

Evidence Appendix

Not applicable.

Related Proceedings Appendix

Not Applicable.

Respectfully submitted,

Daniel J. Bedell
Reg. No. 30,156

SMITH-HILL & BEDELL, P.C.
16100 N.W. Cornell Road, Suite 220
Beaverton, Oregon 97006

Tel. (503) 574-3100
Fax (503) 574-3197
Docket: CRED 2779